PCT/JP2003/015165

Translation

PATENT COOPERATION TREATY

PCT

INTERNATIONAL PRELIMINARY EXAMINATION REPORT

(PCT Article 36 and Rule 70)

Applicant's or agent's file reference NT1369PCT	FOR FURTHER ACTION See Notification of Transmittal of International Preliminary Examination Report (Form PCT/IPEA/416)	
International application No. PCT/JP2003/015165	International filing date (*day/month/year*) 27 November 2003 (27.11.2003)	Priority date (*day/month/year*) 28 November 2002 (28.11.2002)
International Patent Classification (IPC) or national classification and IPC G06F 12/06, G11C 11/401		
Applicant RENESAS TECHNOLOGY CORP.		

1. This international preliminary examination report has been prepared by this International Preliminary Examining Authority and is transmitted to the applicant according to Article 36.

2. This REPORT consists of a total of 9 sheets, including this cover sheet.

☐ This report is also accompanied by ANNEXES, i.e., sheets of the description, claims and/or drawings which have been amended and are the basis for this report and/or sheets containing rectifications made before this Authority (see Rule 70.16 and Section 607 of the Administrative Instructions under the PCT).

These annexes consist of a total of _____ sheets.

3. This report contains indications relating to the following items:

- I ☒ Basis of the report
- II ☐ Priority
- III ☐ Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
- IV ☐ Lack of unity of invention
- V ☒ Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
- VI ☒ Certain documents cited
- VII ☐ Certain defects in the international application
- VIII ☐ Certain observations on the international application

Date of submission of the demand	Date of completion of this report
27 November 2003 (27.11.2003)	28 March 2005 (28.03.2005)
Name and mailing address of the IPEA/JP Facsimile No.	Authorized officer Telephone No.

INTERNATIONAL PRELIMINARY EXAMINATION REPORT

International application No.
PCT/JP2003/015165

I. Basis of the report

1. With regard to the elements of the international application:*

☒ the international application as originally filed

☐ the description:

pages _____, as originally filed
pages _____, filed with the demand
pages _____, filed with the letter of _____

☐ the claims:

pages _____, as originally filed
pages _____, as amended (together with any statement under Article 19
pages _____, filed with the demand
pages _____, filed with the letter of _____

☐ the drawings:

pages _____, as originally filed
pages _____, filed with the demand
pages _____, filed with the letter of _____

☐ the sequence listing part of the description:

pages _____, as originally filed
pages _____, filed with the demand
pages _____, filed with the letter of _____

2. With regard to the **language**, all the elements marked above were available or furnished to this Authority in the language in which the international application was filed, unless otherwise indicated under this item.
These elements were available or furnished to this Authority in the following language _____ which is:

☐ the language of a translation furnished for the purposes of international search (under Rule 23.1(b)).

☐ the language of publication of the international application (under Rule 48.3(b)).

☐ the language of the translation furnished for the purposes of international preliminary examination (under Rule 55.2 and/or 55.3).

3. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, the international preliminary examination was carried out on the basis of the sequence listing:

☐ contained in the international application in written form.

☐ filed together with the international application in computer readable form.

☐ furnished subsequently to this Authority in written form.

☐ furnished subsequently to this Authority in computer readable form.

☐ The statement that the subsequently furnished written sequence listing does not go beyond the disclosure in the international application as filed has been furnished.

☐ The statement that the information recorded in computer readable form is identical to the written sequence listing has been furnished.

4. ☐ The amendments have resulted in the cancellation of:

☐ the description, pages _____

☐ the claims, Nos. _____

☐ the drawings, sheets/fig _____

5. ☐ This report has been established as if (some of) the amendments had not been made, since they have been considered to go beyond the disclosure as filed, as indicated in the Supplemental Box (Rule 70.2(c)).**

* *Replacement sheets which have been furnished to the receiving Office in response to an invitation under Article 14 are referred to in this report as "originally filed" and are not annexed to this report since they do not contain amendments (Rule 70.16 and 70.17).*

** *Any replacement sheet containing such amendments must be referred to under item 1 and annexed to this report.*

INTERNATIONAL PRE[redacted]INARY EXAMINATION REPORT

Inter[redacted]al application No.
PCT/JP 03/15165

V. **Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement**

1. Statement

Novelty (N)	Claims	1-78	YES
	Claims		NO
Inventive step (IS)	Claims	1-41, 49, 51, 54, 61-66, 69-72, 75-76	YES
	Claims	42-48, 50, 52-53, 55-60, 67-68, 73-74, 77-78	NO
Industrial applicability (IA)	Claims	1-78	YES
	Claims		NO

2. Citations and explanations

Documents cited in the international search report:

Document 1: JP 2001-344967 A (Hitachi, Ltd.), 14 December 2001, entire text, all drawings, & US 2001/0046167 A1, & KR 2001/107538 A

Document 2: JP 5-299616 A (Hitachi, Ltd.), 12 November 1993, paragraphs [0027], [0105]-[0108], fig. 14, & EP 566306 A2

Document 3: JP 8-305680 A (Matsushita Electric Industrial Co., Ltd.), 22 November 1996, entire text, all drawings

Document 4: JP 2002-251884 A (Toshiba Corp.), 6 September 2002, entire text, all drawings, & US 2002/0114178 A1

Claims 1 to 41, 69 to 72, and 75 and 76

The inventions described in claims 1 to 41, 69 to 72, and 75 and 76 involve an inventive step relative to documents 1 to 4.

Documents 1 to 4 do not disclose a memory module that includes a non-volatile memory, DRAM, SRAM, and a control circuit for performing access operations between the aforementioned non-volatile memory and the aforementioned DRAM and SRAM, wherein a DRAM interface for accessing the aforementioned DRAM from a point external to

the memory module and an SRAM interface for accessing the aforementioned SRAM from a point external to the memory module are separately provided; meanwhile, this configuration produces the advantageous effect of allowing the simultaneous execution of DRAM access and SRAM access.

Claim 42

The invention described in claim 42 does not involve an inventive step in the light of document 1 and document 2.

The decision as to whether to make an interface with an external point a DRAM interface or an SRAM interface is merely a feature fittingly determined by a person skilled in the art, and a person skilled in the art could easily change the SRAM interface of the memory module disclosed in document 1 to a DRAM interface, as disclosed in document 2.

Claims 43 to 45

The invention described in claims 43 to 45 does not involve an inventive step in the light of document 1 and document 2.

As disclosed in document 2, the transfer of non-volatile memory data to SRAM or DRAM when power is turned on is nothing more than a conventional means.

Claims 46 and 47

The invention described in claims 46 and 47 does not involve an inventive step in the light of document 1 and document 2.

Performing error correction or address alternate processing as needed when transferring data does not pose any particular difficulty.

Claim 48

The invention described in claim 48 does not involve an inventive step in the light of document 1, document 2, and document 3.

As disclosed in document 3, maintaining a boot program in non-volatile memory does not pose any particular difficulty.

Claims 49 and 51

The invention described in claims 49 and 51 involves an inventive step relative to documents 1 to 4.

Documents 1 to 4 do not disclose the maintaining of transfer range data in non-volatile memory; meanwhile, this configuration produces the advantageous effect of allowing the transfer of data from a specified address region without specifying the transfer range from an external point.

Claim 50

The invention described in claim 50 does not involve an inventive step in the light of document 1 and document 2.

Making the memory capacity of non-volatile memory and DRAM approximately the same when performing backup of DRAM with non-volatile memory is merely standard practice.

Claims 52 and 53

The invention described in claims 52 and 53 does not involve an inventive step in the light of document 1 and document 2.

Stopping a DRAM data-holding operation internally when the data-holding operation is executed in DRAM from an external point is known in the art, as disclosed in document 2 (paragraph [0108]).

Claim 54

The invention described in claim 54 involves an inventive step relative to documents 1 to 4.

Documents 1 to 4 do not disclose a configuration wherein access from a point external to a memory module is given first priority, a data-holding operation in DRAM is given second priority, and data transfer between non-volatile memory and SRAM and DRAM is given third priority; meanwhile, this configuration produces the advantageous effect of allowing data-holding in DRAM without delaying access from an external point.

Claims 55 to 57

The invention described in claims 55 to 57 does not involve an inventive step in the light of document 1 and document 2.

Using synchronous DRAM for DRAM and NAND-type flash memory or AND-type flash memory for non-volatile memory does not pose any particular difficulty.

Claim 58

The invention described in claim 58 does not involve an inventive step in the light of document 1 and document 2.

Performing error detection and correction or address alternate processing in non-volatile memory as needed does not pose any particular difficulty.

Claims 59 and 60, claim 67

The invention described in claims 59 and 60 and claim 67 does not involve an inventive step in the light of document 1 and document 2.

Using a NAND configuration or an AND configuration for the configuration of a non-volatile memory array does not pose any particular difficulty.

Claims 61 to 63

The invention described in claims 61 to 63 involves an inventive step relative to documents 1 to 4.

Documents 1 to 4 do not disclose a feature wherein DRAM is provided with a plurality of memory interfaces; meanwhile, this configuration produces the advantageous effect of allowing simultaneous execution of access from an external point and internal transfer.

Claims 64 to 66

The invention described in claims 64 to 66 involves an inventive step relative to documents 1 to 4.

Documents 1 to 4 do not disclose a feature wherein DRAM is provided with a control circuit that allows the independent execution of access to non-volatile memory; meanwhile, this configuration produces the advantageous effect of allowing DRAM to independently access non-volatile memory.

Claim 68

The invention described in claim 68 does not involve an inventive step in the light of document 1 and document 2.

The decision as to whether to make an interface with an external point a DRAM interface or an SRAM interface is merely a feature fittingly determined by a person skilled in the art, and a person skilled in the art could easily conceive of changing the SRAM interface of the memory module disclosed in document 1 to a DRAM interface, as disclosed in document 2, and transferring data between an information processing device and the SRAM and DRAM in the memory module through the DRAM interface.

Claims 73 and 74

The invention described in claims 73 and 74 does not involve an inventive step in the light of document 1, document 2, and document 4.

As disclosed in document 4, a person skilled in the art could easily make a DRAM chip include a control circuit and SRAM.

Claims 77 and 78

The invention described in claims 77 and 78 does not involve an inventive step in the light of document 1 and document 2.

Configuring an information apparatus from an information-processing device, a memory device, and an output device does not pose any particular difficulty.

INTERNATIONAL PRELIMINARY EXAMINATION REPORT

International application No.
PCT/JP2003/015165

VI. Certain documents cited

1. Certain published documents (Rule 70.10)

Application No. Patent No.		Publication date *(day/month/year)*	Filing date *(day/month/year)*	Priority date (valid claim) *(day/month/year)*
JP 2002-366429 A	E,Y	20 December 2002 (20.12.2002)	11 June 2001 (11.06.2001)	
JP 2003-6041 A	E,Y	10 January 2003 (10.01.2003)	20 June 2001 (20.06.2001)	
JP 2003-297082 A	E,Y	17 October 2003 (17.10.2003)	01 April 2002 (01.04.2002)	
JP 2004-102781 A	E, Y	02 April 2004 (02.04.2004)	11 September 2002 (11.09.2002)	
JP 2004-102508 A	E, Y	02 April 2004 (02.04.2004)	06 September 2002 (06.09.2002)	
JP 2004118544 A	E, Y	15 April 2004 (15.04.2004)	26 September 2002 (26.09.2002)	

2. Non-written disclosures (Rule 70.9)

Kind of non-written disclosure	Date of non-written disclosure *(day/month/year)*	Date of written disclosure referring to non-written disclosure *(day/month/year)*